Photon-Induced Negative Capacitance in Metal Oxide Semiconductor Structures

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***Abstract*—Design and fabrication of photon-induced negative capacitance is presented. The capacitor is implemented using Silicon on Insulator Metal Oxide Semiconductor platform, where the gate dielectric is made of a nonferroelectric material. Operating at room temperature, when the device is illuminated, in depletion mode the total capacitance grows in magnitude to values larger than the geometrical capacitance. We believe this is caused by the trap states existing at the interface of dielectric and semiconductor layers, and present the supporting modeling results. Using our model, we investigate the role of the trap density and light intensity, as well as the device geometry such as gate-ground position and the thickness of the silicon layer. Our model shows the depletion capacitance can grow to values more than three times larger than the geometrical capacitance.**

***Index Terms*—Interface trap states, negative capacitance, MOS capacitor, photo-generation.**

I. Introduction

NEGATIVE capacitance has been observed in three classes of devices: forward biased rectifying devices, two dimensional electron/hole gases where exchange-correlation determines the physics, and the ubiquitous metal-oxide-semiconductor (MOS) devices with ferroelectric gate dielectrics. Reports of the observation of negative capacitance in a broad family of rectifying devices include metal-semiconductor junctions [1], organic light emitting diodes [2]–[4], solar cells [5], and quantum well infrared photo-detectors [6]. These capacitors have a large leakage current, and hence do not have purely complex impedance, which makes them highly dissipative and unsuitable for low power device applications.

In the second group, the two dimensional electron or hole gas based devices, the total capacitance of a parallel plate capacitor in the quantum limit is a series combination of the geometrical capacitance and four other capacitances, which originate from the electrons' kinetic energy, exchange energy, correlation energy, and from the coupling energy of electrons and phonons [7], [8]. Since the exchange and the correlation capacitances can be negative, the total capacitance can take values larger than the geometrical capacitance.

Experimentally, a large capacitance has been observed in two-dimensional hole [9] and electron [10] gases, carbon nanotubes [11], and in graphene in the presence of magnetic fields [12], [13], due to negative compressibility arising from the quantum mechanical (exchange-correlation) interaction energy. Negative capacitance corrections have also been proposed in recent experiments involving single layer graphene. Reference [14] proposed that the negative capacitance in Ag-adsorbed single-layer graphene capacitors is due to an interplay between kinetic energy quenching and Coulomb energy variation. While [10] and [14] measure the quantum mechanically induced negative capacitance at liquid helium temperatures, [9] reports it at room temperature.

The third class of devices where negative capacitances have been proposed and observed are MOS structures with a novel modification to include a ferroelectric gate dielectric [15]. The polarization versus electric field in ferroelectric materials exhibits a negative slope. This translates into a negative charge versus voltage curve, and hence a negative capacitance. As a result, it is possible to design low power devices because subthreshold slopes smaller than 60 mV/dec are feasible in negative capacitance based MOS transistors [15], [16].

In this manuscript, we propose a new photon induced effect which leads to a negative capacitance in MOS capacitors at room temperature. Before discussing the underlying physics, we briefly illustrate how the negative capacitance manifests itself in MOS geometry. Considering a MOS capacitor biased in depletion mode, its total capacitance is a series combination of the geometrical oxide capacitance C_{ox} and the semiconductor capacitance C_s

$$C_{\rm tot}^{-1} = C_{\rm ox}^{-1} + C_s^{-1} \tag{1}$$

where $C_{\rm tot}$ denotes the total capacitance. The geometrical capacitance is dependent on the permittivity and thickness of the oxide, and can take only positive values (unless as in [15] and [16], a ferroelectric material is used to obtain a negative slope for polarizability versus electric filed). The semiconductor capacitance depends on the semiconductor properties such as its bandgap, density of states and doping, as well as the gate bias. The trap states at the oxide-semiconductor interface can also contribute to the semiconductor capacitance. Under such condition, it is possible for C_s to take negative values, causing the total capacitance $C_{\rm tot}$ to be larger than the geometrical capacitance $C_{\rm ox}$.

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The total capacitance is also a function of the gate voltage V_G and the surface potential ψ_s,

$$C_{\rm tot} = C_{\rm ox}\left(1 - \frac{d\psi_s}{dV_G}\right). \quad (2)$$

According to equation (2), if $d\psi_s/dV_G$ can be made negative, a total capacitance larger than the oxide capacitance is possible. While in an ideal MOS capacitor $d\psi_s/dV_G$ is positive and smaller than unity, we explore a method to induce negative $d\psi_s/dV_G$ by using photons. Theoretically it is possible to fill the traps at the oxide-semiconductor interface by photo-excitation of valence band electrons. If the number of the filled traps is large enough, it can force the surface potential to decrease (instead of increase), causing the total capacitance to grow larger than the geometrical capacitance.

II. Device Fabrication

We fabricated the MOS capacitors on (100) Silicon on Insulator (SOI) wafers, with the top silicon and buried oxide layers of 340 nm and 1 μm, respectively. The silicon layer is p-type with doping density of about 6×10^{14} to 9.5×10^{14} cm^{-3}. The active region was created by dry etching the top silicon layer into mesas, using a negative electron beam resist (Ma-N 2400) as the etch mask. After dry etching, the resist was removed and the samples were cleaned by Piranha cleaning process (H_2SO_4: H_2O_2 4:1). Next the native oxide layer was etched away in a buffered Hydro Fluoric acid mixture (BHF, 10:1), and 25 nm of Aluminum Oxide (Al_2O_3) was deposited over the exposed silicon surface by means of plasma assisted Atomic Layer Deposition at 300 °C.

In order to fabricate the ground contact, we created appropriate windows in the Al_2O_3 layer using electron beam lithography and then etched the Al_2O_3 layer in a BHF mixture. We then deposited 250 nm of Al, followed by the lift off process. The process of fabricating the gate contact was similar, with the exception of wet etching the dielectric layer. We annealed the samples in forming gas (N_2:H_2, 90:10) at a temperature of 425 °C for 30 min. The inset of Fig. 1 shows an optical image of a MOS capacitor.

We obtained the quasi-static capacitance-voltage (QSCV) characteristic of the MOS capacitor by using an Agilent 4155C semiconductor parameter analyzer. A 405 nm laser diode at various intensities was used to illuminate the device during measurements. The representative results are shown in Fig 1. Under dark, no peak was observed in the CV curve (see Fig. 1). Under illumination and in depletion mode, we observed a peak that appeared and grew with increase in light intensity. As shown in the figure, the peak is larger than the capacitance value in accumulation region at 7.2 mW/cm^2, indicating the negative capacitance mechanism. We note that the fluctuations in the graph of Fig. 1 are mostly due to the noise coming from the unstably mounted laser source. The same capacitor shows a much cleaner CV curve when illuminated with microscope light. We also emphasise that the capacitance peak in depletion seen in our data consists of more than 25 data points, demonstrating a systematic increase/decrease of capacitance.

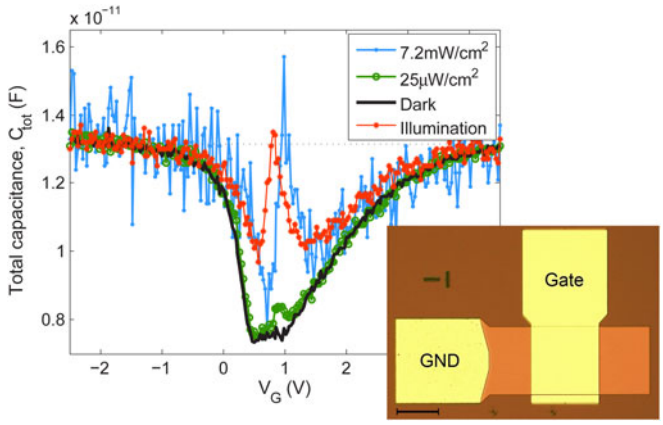


Fig. 1. QSCV graph at various light intensities. Graph is based on raw data; and "Illumination" represents the response to the microscope light (Intensity not recorded). Inset shows a MOS capacitor fabricated over SOI substrate. The scale bar is 50 μm.

III. Modeling and Discussion

To illustrate the observed phenomenon, we consider p-type silicon with acceptor type interface traps, which are neutral when empty, and negatively charged when filled. These states do not influence the surface potential in accumulation mode as they are empty and neutral. Sweeping the gate voltage towards depletion leads to migration of the majority carriers (holes) away from the oxide-semiconductor interface, and attraction of electrons towards the interface, which is accompanied by the lowering of the conduction and valence bands at the interface. With increase in gate voltage, the traps at the interface start to fall below the Fermi level and fill up. The channel would therefore need to be less depleted in response to the gate voltage increase, as the filled trap states provide a negative charge. This would drop the rate at which the surface potential increases with gate bias, when compared to a capacitor without interface traps. Under this circumstance, if a large number of electrons fill the interface trap states, one may be able to force the surface potential to decrease (instead of increasing) in response to an increase in the gate voltage. In our device, this large number of electrons is provided by photo excitation of electrons from the valence band.

We model the capacitor by considering the SOI prototype of Fig. 2(a), where the top silicon layer is 350 nm thick, with a doping concentration of 10^{15} cm^{-3} (p-type). The gate dielectric layer is assumed to be aluminum oxide, with thickness and permittivity of 25 and 7nm, respectively. Our model is built using the Poisson and drift-diffusion framework, with the inclusion of the interface trap states. The trap states at the silicon-dielectric interface are modeled by using the bandgap interface defect model [17] that approximates the density of the acceptor- and donor-like states by a Gaussian and an exponential distribution. The numerical values for distributions are summarized in Table I. These values and the gate work function are determined so as to match the CV under dark condition in the experiments and are close to the values reported in literature for a silicon-alumina interface [18].

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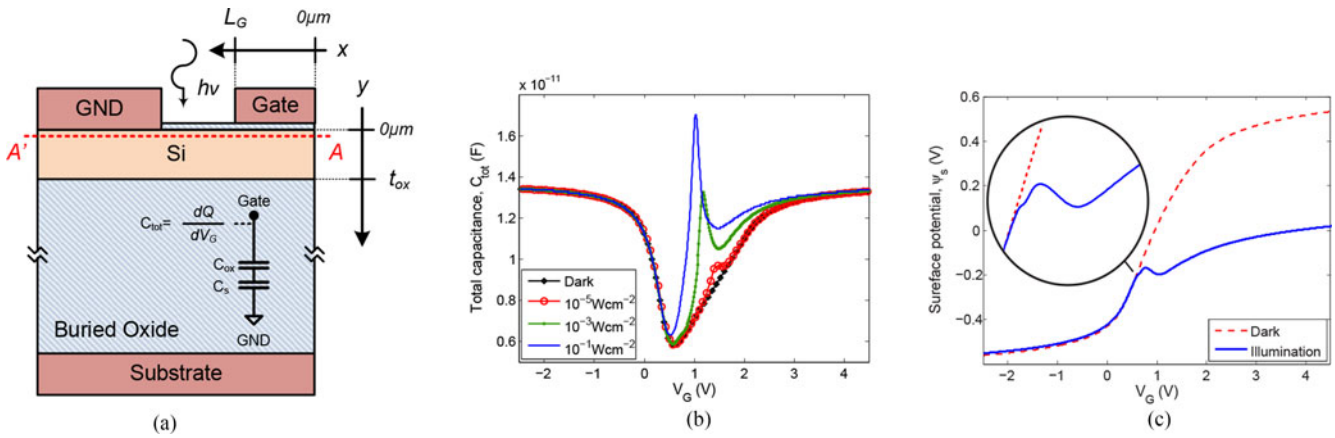


Fig. 2. (a) Two dimensional SOI MOS capacitor. (b) QSCV data of the device in (a), calculated using the Poisson's and drift-diffusion equations. $\lambda = 405$nm for illumination results. (c) Surface potential at point $x = 50$ μm underneath the gate, under dark and illumination conditions.

TABLE I
PARAMETERS OF THE BANDGAP INTERFACE DEFECT MODEL

Defect type	Gaussian distribution			Exponential (tail) distribution	
	Energy that corresponds to the peak (eV)	Total density of states (cm^{-2}/eV)	The characteristic decay energy (eV)	Density of trap states at the band edge (cm^{-2}/eV)	The characteristic decay energy (eV)
Acceptor	0.35	10^{12}	0.4	2×10^{13}	0.12
Donor	0.6	10^{6}	0.3	2×10^{12}	0.2

The density of the filled traps depends on the overall trap density, and also on the trap ionization probability. The probability of an acceptor type interface trap being occupied at energy E_t is [17], [19]:

$$F_{tA} = \frac{\upsilon_n \sigma_{An} n + \upsilon_p \sigma_{Ap} n_i e^{\left(\frac{E_i - E_t}{kT}\right)}}{\upsilon_n \sigma_{An} n + \upsilon_p \sigma_{Ap} p + \upsilon_n \sigma_{An} n_i e^{\left(\frac{E_t - E_i}{kT}\right)} + \upsilon_p \sigma_{Ap} n_i e^{\left(\frac{E_i - E_t}{kT}\right)}}. \quad (3)$$

In equation (3), n, p, υ_n and υ_p denote the electron and hole concentration, and the electron and hole thermal velocity, respectively. σ_{An} and σ_{Ap} are the electron and hole capture cross sections, with values of 10^{-16} and 10^{-14} cm^2, respectively. Finally n_i is the intrinsic charge concentration and E_i represents the intrinsic Fermi level. A similar equation is used for the probability of a donor type trap being filled [17], [19].

In order to investigate the capacitor's optical response, a monochromatic light with wavelength of 405 nm is illuminated on the device, as shown in Fig. 2(a). Fig. 2(b) shows the computed QSCV. The trend is in agreement with the experiment. There is no peak at dark. As a result of illumination a peak emerges in the depletion region. The peak value grows as the light intensity increases, and eventually exceeds the value of the geometrical capacitance $C_{\rm ox}$. Calculation of C_s using equation (1) results in negative values for the semiconductor capacitance at regions where $C_{\rm tot}$ is greater than $C_{\rm ox}$.

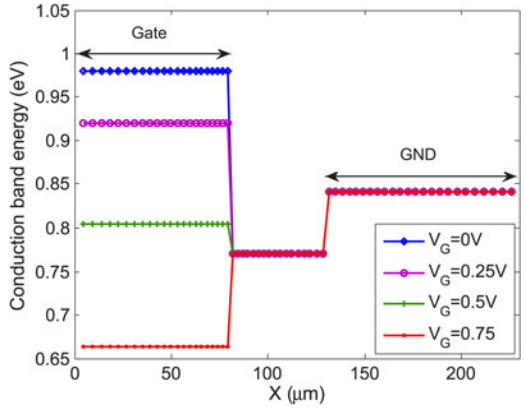


Fig. 3. Conduction band energy, along the channel below the gate dielectric, as shown by dashed lines in Fig. 2(a). Photo-generated carriers can diffuse to the region under the gate only when the gate bias exceeds 0.5 V.

Fig. 2(c) shows the surface potential as a function of gate voltage, obtained at dark and under illumination. The negative slope observed in the surface potential is the origin of the negative capacitance.

It is the gate voltage that determines the location of the capacitance peak. We find using our model that the gate voltage for the capacitance peak in Fig. 2 depends on the lateral potential from gate to ground (GND in Fig. 2(a)) along the channel in the semiconductor. The photo-generated carriers between the gate and ground are effective in providing a large stream of electrons to fill the traps underneath the gate only when the lateral potential profile allows the photo-generated carriers to diffuse underneath the gate. We see in Fig. 3 that for gate voltages larger than 0.5 V, the photo-generated electrons see a potential profile in the channel where transport is feasible. For smaller gate biases, the barrier height is very high; and therefore only few electrons can diffuse towards the areas under the gate. As

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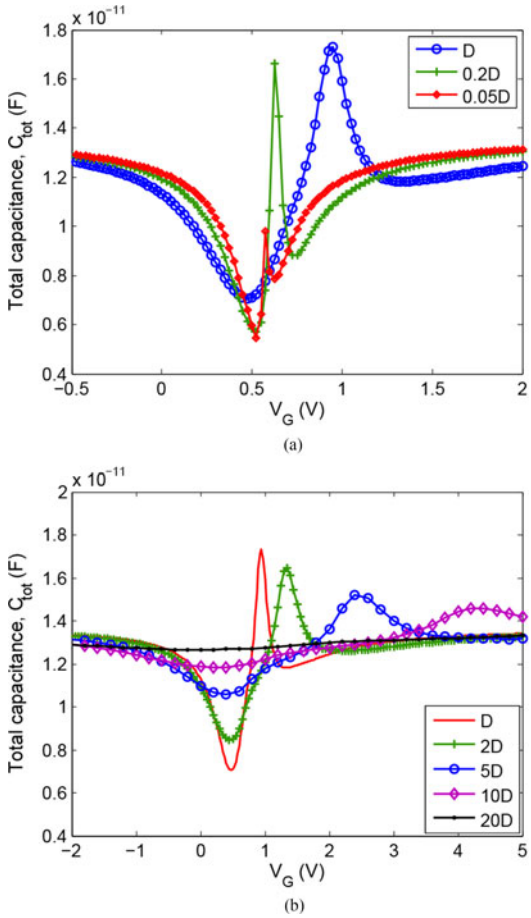


Fig. 4. Role of interface trap density on the photon induced capacitance peak. CV curve versus gate bias, when the trap densities are (a) smaller and (b) larger than the original trap density shown in Table I.

a result, the number of filled interface states does not change in comparison with the dark case. Beyond about $V_G = 0.5$ V, the potential barrier disappears and the number of electrons that reach underneath the gate increases exponentially as the photo-generated carriers diffuse.

The interface trap density plays an important role in modifying the photon induced capacitance peak. To study this, we multiplied the original trap density (D, Table I) by a factor ranging from 0.05 to 20. The change of the CV curve is quite dramatic when the density of the trap states is varied. If the trap density is small, the number of the filled states is not sufficient to force the potential to decrease. In this case, as shown for the factor of 0.05 D in Fig. 4(a), there exists a very small peak in the CV curve (the peak disappears at lower densities). The impact of the interface traps becomes more tangible as the density is increased and the peak in the CV curve grows. However, at higher densities the peak starts to decrease and broaden (Fig. 4(b), D . . . 10D). The reason is that when the interface trap density is high, more traps can be filled by a small change in the surface potential, causing a major part of the charge to be compensated by the filled traps when the gate voltage is changed by ΔV_G. The channel is therefore less depleted for the same bias. Decrease of

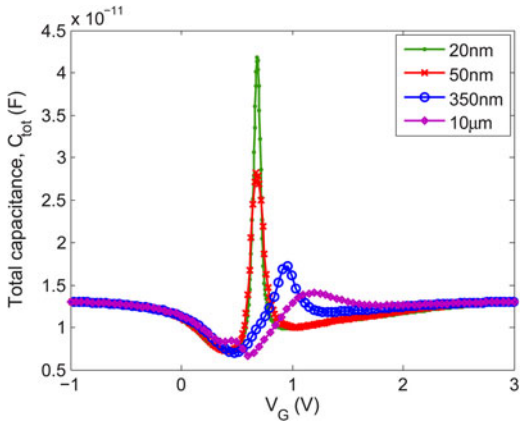


Fig. 5. QSCV curve of the MOS capacitor showing the role of silicon layer thickness on the capacitance peak.

$d\psi_s/dV_G$ results in the capacitance peak to decrease and move toward higher gate biases. An increase in acceptor trap density to much larger values, significantly changes the shape of the CV curve as inversion of the channel cannot occur, and the capacitance remains fixed at the value of the geometrical capacitance. Under this circumstance, a peak in the capacitance is again not seen in the simulations.

The silicon body thickness is an important parameter in determining the magnitude of the negative capacitance. If electrons remain at the bulk section of silicon, the resulting negative charge contributes to compensate for the positive charge variation at the gate. Therefore, it is important for the injected electrons not to accumulate in the bulk, but to reach the interface. On the other hand, due to the geometry of the capacitor, and the position of the gate and ground with respect to each other, injection of the photo-generated electrons is affected by both diffusion (x direction, laterally) and drift (y-direction, vertically) mechanisms. The net movement would be somewhat diagonal. As a result, those electrons that are located farther from the interface (deeper in the silicon layer) take a longer path to reach the surface. Based on this, if the thickness of the silicon layer is reduced, the injected electrons reach the interface after passing a shorter pathway. Therefore, one expects a stronger contribution of the interface states, and hence a stronger negative capacitance. Fig. 5 demonstrates how the silicon thickness impacts the QSCV curves of MOS capacitors. When the silicon thickness ($t_{\rm si}$) is 20 nm, the capacitance shows a peak that is more than three times larger than the geometrical capacitance, $C_{\rm ox}$. The peak decreases as the silicon layer thickness increases.

Although the CV results we have presented in this manuscript are quasi-static, we briefly discuss the frequency response of the structure. Overall, the frequency response would depend on the minority carrier lifetime of the trap states. At low frequencies, the carriers have enough time to settle in the trap states, and as a result we would expect to see a CV curve close to the case of QSCV. At high frequencies (comparable to the inverse of the trap life-time), the photo-generated electrons do not have sufficient time to settle in the trap states and we expect the CV curve under

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illumination to be close to that under dark conditions, with very little or no peak in depletion mode.

IV. Conclusion

In summary, we proposed a new method to induce negative capacitance in MOS capacitor geometry. Our design makes use of the trap states that are present at the interface of the semiconductor and dielectric, underneath the gate. Such states can be filled by carriers that, in our design, are generated as a result of optical illumination. The filled traps provide a source of charge that compensates part of charge required to respond to the change of the gate voltage, and reduce the rate at which surface potential is changed. Negative capacitance occurs if the surface potential decreases in response to the gate voltage increase, when a sufficient stream of carriers is provided. While in a normal MOS capacitor, the depletion mode capacitance is always smaller than the geometrical capacitance, in our design, capacitance values larger than the geometrical capacitance are possible.

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