High-Gain Multiple-Gate Photodetector With Nanowires in the Channel

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***Abstract*—A design of a photodetector with multiple gates and a modified channel, incorporating silicon nanowires, is proposed, and its performance is modeled. Working under lateral bipolar action, the gate/channel geometry increases the device photocurrent in the accumulation mode and leads to photoresponsivities of greater than 10^4 A/W.**

***Index Terms*—Lateral bipolar action, photodetector, photoresponsivity, silicon nanowire (NW).**

I. Introduction

ONE-DIMENSIONAL nanostructures offer features that are potentially important in device application: quantum effects due to their narrow cross section, improved electrostatics, and good transport characteristics along their length. These properties have proved to be useful in laboratory demonstrations of carbon nanotube and silicon nanowire (NW) sensors [1]–[3]. The miniaturized size of 1-D devices provides low power consumption and the ability of integrating arrays of devices in a system. NW arrays are attractive in chemical and biomedical sensors as their ability to work independently provides the opportunity for real-time detection of target molecules [4]. NWs have also been used in building optical switches and photodetectors [5]–[7]. Moreover, there is an interest in incorporating silicon NW-based phototransistors in image sensors, due to their fabrication compatibility with CMOS technology [8], [9].

The small cross section of a single NW limits its optical absorption [10]; however, the nanoscale diameter leads to properties such as polarization anisotropy of absorption in NW-based photodetectors and also the dependence of the absorption spectrum on NW properties such as crystal orientation and doping [5], [11]. Furthermore, there is a solution to compensate the poor absorption of NWs by incorporating the wires into gain-producing devices like avalanche photodiodes [12], photoconductors [7], and phototransistors [9], [13]. These devices [7], [9], [13] are fabricated on silicon-on-insulator (SOI) wafers, as the thin silicon layer facilitates creation of NWs. The device is normally planar: A phototransistor, for example, is similar to metal–oxide–semiconductor (MOS) structures. The device is biased in the lateral bipolar mode in order to produce gain [14]. For this purpose, the source is grounded, and the drain–channel junction is reversed biased. The gate is also biased to prevent the creation of the inversion layer to keep the dark current low. Illumination over the channel generates electron–hole pairs. In a p-type channel, electrons drift in response to the electric field created by the drain bias. The holes, however, cannot pass the potential barrier on the source side and get trapped in the channel. Hole accumulation in the channel lowers the potential barrier, and as a result, a large current flows through the source–drain contacts [14].

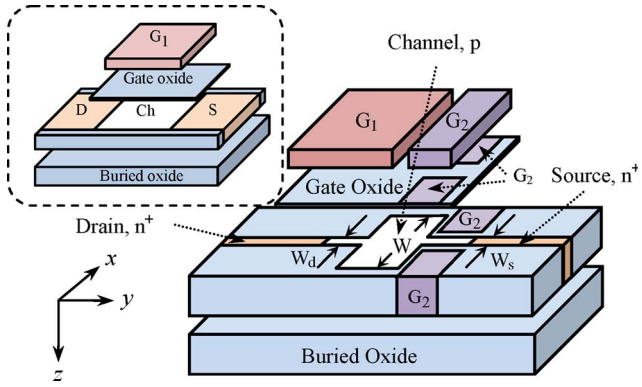


Fig. 1. Multiple-gate NWN photodetector. The widths of the NWs on the source and drain sides, W_s and W_d, are both 60 nm. The total channel length is 1 μm. (Inset) SOI-MOS phototransistor, with a 1-μm-long and 500-nm-wide channel. Light shines through a 0.5×0.5 μm^2 window over the channel. Source and drain contacts are not shown.

This simulation work aims to illustrate how incorporating NWs in a SOI-MOS phototransistor improves the control over the charge flow and increases the device photocurrent. In the proposed geometry, the NWs are integrated in the channel that is electrostatically controlled by a set of two gates. This boosts the photocurrent and leads to photoresponsivities of greater than 10^4 A/W, which is 100 $\times$ larger than the best reported responsivity in an NW-based phototransistor [9].

II. Phototransistor Structure

The proposed device, as shown in Fig. 1, is a SOI-MOS detector with multiple gates. The active region, including n^+ source and drain (doping: 10^{20} cm^{-3}) and a p-type channel (doping: 10^{16} cm^{-3}), is 200 nm thick, located on top of a 200-nm buried oxide. The channel is composed of three regions. The middle part W is under the primary gate G_1 and

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is 500 nm wide. On the two sides, the channel is made of NWs whose widths on the source and drain sides, W_s and W_d, are less than 60 nm ($W_s = W_d \equiv W_{\rm NW}$). The NW on the drain side is 200 nm long and is covered by G_1. The NW on the source side is 300 nm long and is covered by the secondary gate G_2. G_2 covers the front and back of the NW too. The work function of both gates is 4.17 eV. They are separated from the active region underneath by a 20-nm-thick gate oxide. The separation between the gates is 50 nm. Throughout this letter, this device is referred to as *narrow–wide–narrow* (NWN or NWN$_x$), where "x" represents the NW width $W_{\rm NW}$. To fabricate the proposed structure, electron beam lithography followed by dry etching can be used to define the active region. The gate oxide can then be grown by thermal oxidation, followed by gates defined by electron beam lithography and deposition. The last step would be the fabrication of metal contacts by lithography and deposition.

The wide middle of the channel is the main region of absorption. NWs absorb light too, but their primary role is to enhance the photocurrent and lower the dark current as we will explain later. The photoresponse of NWN is compared with that of a SOI-MOS phototransistor [14] with a single gate (inset of Fig. 1). The channel is 500 nm wide; other dimensions and doping profiles of SOI-MOS are similar to those of NWN. The main reason for choosing SOI-MOS as the control is that it generates the largest amount of photocurrent among the family of single-gate phototransistors with the same channel length, and channel width of less than 500 nm [13].

III. Device Simulation

To obtain the electrical characteristics of each device, we solve drift-diffusion equations self-consistently with Poisson's equation using a CAD tool [15]. The optical intensity profile within the device is obtained using the particle-based ray tracing method. We used the absorption coefficient of bulk silicon for both structures. Therefore, the simulation outputs fully show the role of electrostatics in the detector response.

We chose a monochromatic source ($\lambda = 633$ nm) in the results presented here, although our results would qualitatively follow a similar trend for photon energies larger than silicon's bandgap. The number of photons impinging the channel is assumed to be the same for both structures. The dashed lines in Fig. 2(a) represent the drain current versus gate voltage (I_D–V_{G1}) of an NWN$_{60}$ ($W_{\rm NW} = 60$ nm). The results for SOI-MOS are plotted by solid lines. At $V_{G1} = -2$ V, the photocurrent of NWN$_{60}$ is more than seven times larger than that of the SOI-MOS for both intensities. This leads to a photoresponsivity of 1.5×10^4 (1.0×10^4) A/W at the intensity of 0.01 (1.0) mW $\cdot$ cm^{-2} for NWN$_{60}$, while the responsivity of the SOI-MOS is 1.7×10^3 (1.5×10^3) A/W for the same intensities. Photoresponsivity is defined by $I/(P \cdot A)$, where I is the photocurrent and P and A are the light intensity and the incidence area, respectively.

The calculated dark current at room temperature cannot be trusted as it is of the same order as machine precision ($\leq 10^{-16}$ A). We circumvent the problem by calculating the dark current at higher temperatures where it is at least one order of magnitude larger than machine precision. The carrier mobility and semiconductor bandgap are kept fixed as this enables a straightforward interpolation to other temperatures. The simulation data are shown in Fig. 2(b) (Inset: I_D versus V_{G1} at $T = 475$ K). At $V_{G1} = -2$ V, the dark current of NWN$_{60}$ (dashed) is just slightly larger than that of the SOI-MOS (solid).

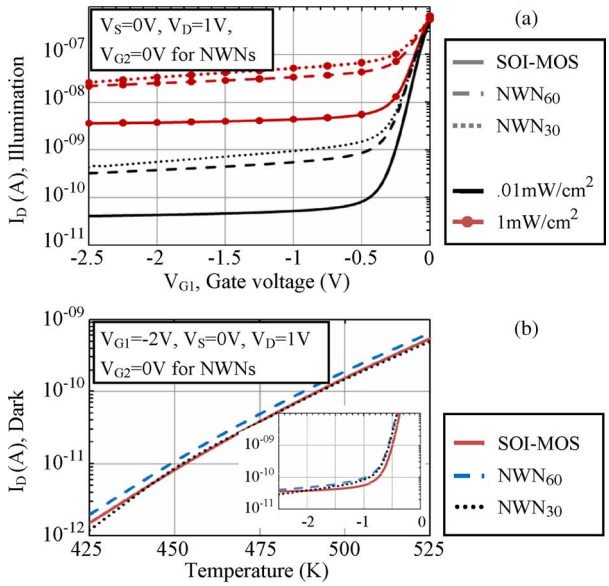


Fig. 2. (a) Drain current versus gate voltage of (dashed) NWN$_{60}$, (solid) SOI-MOS, and (dotted) NWN$_{30}$, under illumination. (b) Dark current versus temperature for (dashed) NWN$_{60}$, (solid) SOI-MOS, and (dotted) NWN$_{30}$. (Inset) I_D (in amperes) versus V_{G1} (in volts) at $T = 475$ K.

TABLE I
PHOTOCURRENT AND DARK CURRENT OF SOME NWN STRUCTURES

NW width, (nm) W_s=W_d	Photocurrent (A) at intensity = .01mW/cm^2	Dark current (A) at T=475K
100	2.6x10^{-10}	5.7x10^{-11}
60	3.7x10^{-10}	4.9x10^{-11}
30	5.5x10^{-10}	3.9x10^{-11}
10	7.7x10^{-10}	2.3x10^{-11}

Note: All data is extracted at V_{G1}=-2V.

Further investigations show that the performance of NWN can be optimized by reducing the NW width on both sides. This is shown in Fig. 2(a) and (b) for an NWN with $W_{\rm NW} = 30$ nm (NWN$_{30}$). Simulated data of a few NWN structures are also summarized in Table I, and one can see that the NWN with $W_{\rm NW} = 10$ nm shows the best results. NW widths below 10 nm are out of the scope of this letter, as the quantum mechanical effects begin to become important.

IV. Discussion

The improved performance of the new device is attributed to better control of the energy band in the NWs when compared to wider channels. As shown in Fig. 3(a), the potential barrier of NWN (both 30 and 60) is lower than that of the SOI-MOS. The current increases exponentially with reducing the barrier height. It also linearly depends on the NW width $W_{\rm NW}$. The lower barrier of NWN therefore overcomes the smaller channel width and results in a larger photocurrent. The

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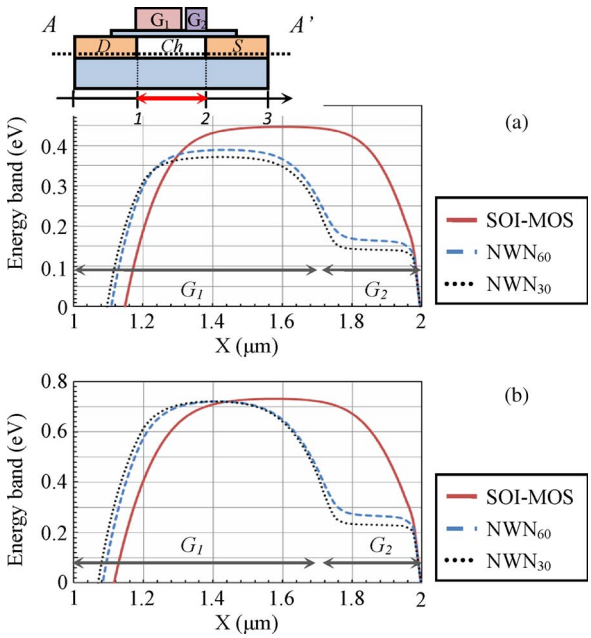


Fig. 3. Energy band diagrams of (dashed) NWN_{60}, (solid) SOI-MOS, and (dotted) NWN_{30}, along cutline AA' for channel region, under (a) light and (b) dark. $V_S = 0$ V, $V_D = 1$ V, and $V_{G1} = -2$ V. For NWN, $V_{G2} = 0$ V.

low potential barrier of NWN is created by the zero biased G_2 that tends to deplete the NW underneath from the majority carriers [Fig. 3(a)]. The photogenerated holes are thus forced to either diffuse into the source or migrate toward the channel under G_1. The latter increases the concentration of holes in a smaller area. To compensate this, the barrier is lowered more, allowing a larger flow of electrons. Moreover, the NW on the source end acts like a "*funnel*"; its small cross-sectional area prevents the holes from diffusing into the source as rapidly as those in SOI-MOS.[1] The lateral bipolar action is then enhanced, causing a larger photocurrent. The dotted curve in Fig. 3(a) is the energy band of NWN_{30}. The narrower wire on the source side enhances the effect of G_2 on pulling the barrier down, causing a larger photocurrent compared with NWN_{60} [Fig. 2(a)].

The barrier lowering by G_2 can come at the price of a high dark current however. We have suppressed this by the aid of the primary gate G_1 and also the channel geometry. As shown in Fig. 3(b), the barrier of the NW underneath G_1 is controlled more effectively by the negative gate in comparison with the SOI-MOS channel. The high barrier and the wire's small cross section keep the dark current low for both NWN devices. In addition, as the NW width on the drain side is decreased (from 60 to 30 nm), G_1 controls the barrier more effectively and decreases the dark current as shown in Fig. 2(b).

Since about 8% of photons are absorbed in the 0.2-μm-thick silicon, NWN is obviously not optimized in terms of external quantum efficiency (EQE). A thicker active region improves EQE, but it degrades the electrostatics if the thickness exceeds a limit. While solutions like reflective mirrors are possible, we would like to emphasize that the design concept is general and can be applied to semiconductors other than silicon.

Finally, ignoring the surface recombination effects that depend on the fabrication process, thermal noise dominates the dark current shot noise in both SOI-MOS and NWN. It is $1.8 \times 10^{-11} B^{1/2}$ A, assuming a 50-Ω load and receiver bandwidth of B. This leads to a lower noise equivalent power in NWN considering its larger responsivity.

V. Conclusion

We have proposed a new device geometry with two gates and a modified channel to increase the photocurrent of the NW-based device in the accumulation mode. This geometry can provide responsivities of greater than 10^4 A/W.

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