Influence of defects on nanotube transistor performance

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We study the effect of vacancies and charged impurities on the performance of carbon nanotube transistors by self-consistently solving the three-dimensional Poisson and Schrödinger equations. We find that a single vacancy or charged impurity can decrease the drive current by more than 25% from the ballistic current. The threshold voltage shift in the case of charged impurities can be as large as 40 mV. © *2006 American Institute of Physics*. [DOI: 10.1063/1.2211932]

Carbon nanotube field effect transistors (CNTFETs) have excellent device characteristics and are candidates for future digital switches and rf transistors.[1–5] Simple circuits based on CNTFETs have already been demonstrated.[6] An important consideration in the design and reliability of circuits is the role of defects, impurities, and parameter fluctuations in affecting the device characteristics. In this letter, we investigate how vacancies and charged impurities affect the device characteristics of CNTFETs. Vacancies arise in graphite at low concentrations during growth and are part of the thermal equilibrium concentration.[7,8] They are believed to be the predominant defects on irradiated graphite surfaces and CNTs (Refs. 9–12) and stable on long time scale. Charged impurities usually consist of ions, molecules, alkali metals, or dopants that exchange charge with the CNT or electrostatically interact with the nanotube.[13–16]

The model device considered consists of a (13,0) zigzag CNT, with 1 nm diameter and 0.8 eV band gap (Fig. 1). The length of the undoped channel and source/drain extension regions are 25 and 22.5 nm, respectively. The source/drain regions are doped uniformly with $N_D=10^9$ dopants/m. The surrounding gate oxide is a 4 nm thick HfO_2 high κ dielectric material ($\kappa=16$), whereas the interior of the CNT is vacuum ($\kappa=1$). We chose a gate work function that produces flatband conditions at $V_G=-E_g/4$, where E_g is the band gap of the CNT ($\Phi_{\text{gate}}=\Phi_{\text{CNT}}+E_g/4$). The applied drain ($V_D$) and gate ($V_G$) biases vary from 0 to 0.45 V, which provide an excellent $I_{\text{on}}/I_{\text{off}}=10^5$ ratio and drive current of $I_{\text{on}}=20$ μA, which are comparable to experimentally reported CNTFET values.[2] Our simulator includes a full three-dimensional (3D) treatment of electrostatics, and is based on real space nonequilibrium Green's function (NEGF) technique within the nearest neighbor π-orbital approximation.[17,18] To model the vacancy, we set the on-site potential to 10^6 eV at the carbon vacancy site, which ensures that a channel electron is effectively repelled from the location of the vacancy.[19]

We find that the vacancy creates a localized state in the band gap and a reduction of the transmission probability in both the conduction and valence bands. The reduction in the transmission probability based on π-orbital model has been confirmed by nonorthogonal extended Hückel calculations using sp^3 orbitals for each carbon. The localized state in the band gap appears in the Hückel calculations too; however, it is slightly shifted towards the valence band. This behavior is verified experimentally[20] and has also been observed through *ab initio* calculations for metallic tubes with relaxed geometry.[21] In this study we do not include effects of structure relaxation due to a vacancy and place it in the middle of the channel.

There are two reasons for the change in the transport characteristics due to a vacancy. (i) Change in bonding between the vacancy and its three nearest neighbors. This causes a reduction in the transmission even in the absence of self-consistency. (ii) Localized states created by the vacancy. When the transistor is in the off state, the conduction band edge (E_C) in the channel is 0.2 eV above the source Fermi level, and the channel is almost empty of charge. As a result, the vacancy changes the transport characteristics mainly through a reduction in the transmission probability [effect (i) above]. When the transistor is turned on ($V_G=V_D=0.4$ V), the localized state in the band gap gets partially filled [effect (ii) above], which changes the potential profile and carrier occupancy in the channel. The combination of transmission reduction and the slight increase of the source injection barrier decrease the drive current by 28% from 18.5 to 13.5 μA [Fig. 2(c)]. We note that a 12 mV shift in the threshold voltage (V_t) is also observed. This shift, however, is responsible for only approximately 8% of the total 28% reduction in I_{on}.

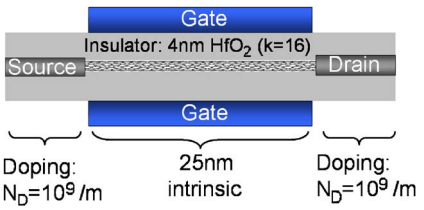


FIG. 1. (Color online) Two-dimensional (2D) cross section of the device. The device is a 3D coaxial CNTFET with 25 nm channel length and 22.5 nm source/drain extensions doped to 10^9 dopants/m. The channel is a semiconducting (13,0) zigzag CNT with 1 nm diameter and 0.8 eV band gap. The gate oxide is assumed to be 4 nm thick HfO_2 with dielectric constant $\kappa=16$.

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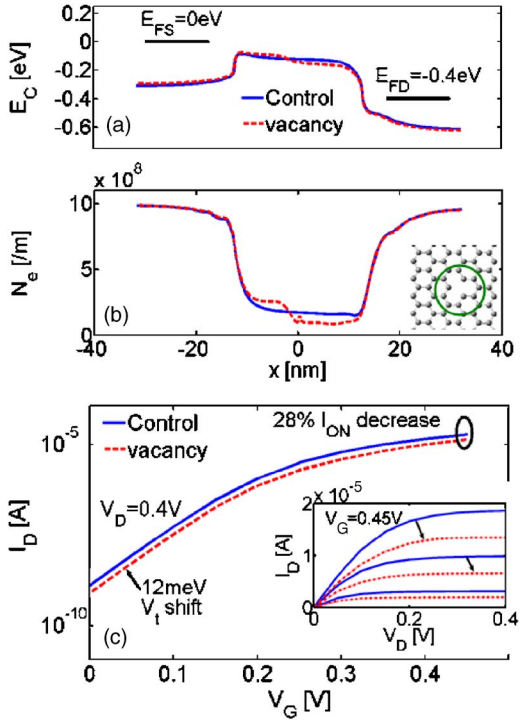


FIG. 2. (Color online) Effect of the vacancy on the electronic properties of the CNTFET. (a) The conduction band of the control vs vacancy defected CNT at V_G=0.4 V and V_D=0.4 V. (b) The carrier distribution along the channel of the two devices under bias conditions as in (a). (c) The I_D-V_G characteristics at V_D=0.4 V. Inset: the I_D-V_D for V_G=0.45, 0.35, and 0.25 V.

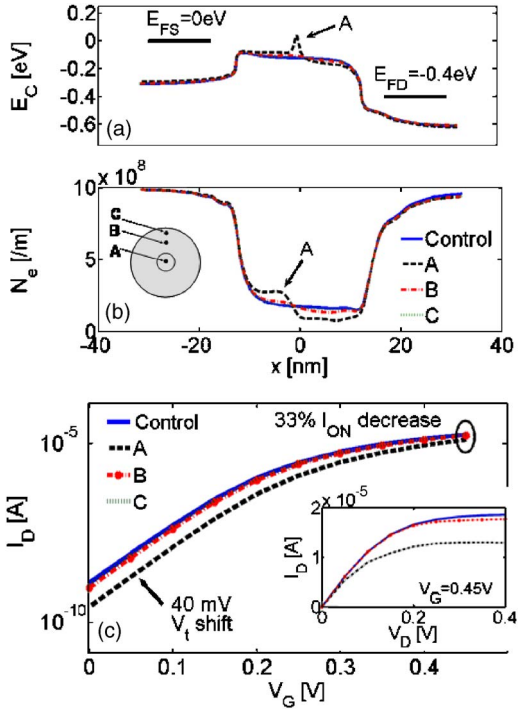


FIG. 3. (Color online) Effect of a negatively charged impurity in different locations of the device. The charged impurity is placed (A) in the middle of the CNT, (B) in the middle of the oxide, and (C) near the gate electrode. (a) The conduction band of the control vs the different charged impurity cases at V_G=V_D=0.4 V. (b) The carrier distribution along the channel for the impurity locations (A)–(C) and the same bias conditions as in (a). (c) The I_D-V_G characteristics for V_D=0.4 V. Inset: I_D-V_D for V_G=0.45 V.

We also considered the case where the vacancy sits near the source and drain ends, and find that the drive current decreases by a similar amount, indicating that the decrease in drive current is independent of the vacancy location.

We next investigate the effect of a negatively charged impurity having charge $-|q|$, where q is the charge of an electron. Three different locations of the impurity are considered: (A) the interior of the CNT, (B) the middle of the oxide, and (C) the top of the oxide, 0.5 nm from the gate electrode [inset of Fig. 3(b)]. We assume that the effect of the impurity on the device arises through electrostatic interactions, and ignore any minor structure deformations due to the impurity.[16] We find that case (A) gives rise to a large scattering center in the conduction band as shown in Fig. 3(a). Similar to the case of the localized state with a vacancy, electrons traveling from the source to the drain get reflected from this barrier and pileup/deplete to the left/right of the impurity [Fig. 3(b)]. The comparison to the case of a vacancy is interesting. While the drive current is reduced by about 33%, similar to the case of the vacancy, there is now a large shift in the threshold voltage by about 40 mV. For an operating bias of 0.4 V, the threshold voltage shift is about 10%, a magnitude that can lead to large I_{off} variations. In comparison to case (A), the drive current and threshold voltage are affected very little in cases (B) and (C) (5% and 0.5% reductions, respectively). This behavior can be attributed to an effective screening of the impurity by the surrounding gate electrode, enhanced by the high κ dielectric of the gate insulator.

Finally, we investigate the effect of a positively charged impurity placed at the same locations as in Fig. 3(b). While a negatively charged impurity in the center of the CNT creates a large barrier in the conduction band, a positive impurity creates a large potential well as shown in Fig. 4(a). The carrier density in the channel [Fig. 4(b)] slightly oscillates, and electrons are attracted around the positive impurity site in the middle of the channel. The top of the barrier, however, is not affected significantly in this case, and as a result the drive current deceases by only 11% as shown in Fig. 4(c). Quantum mechanical scattering from a potential well is weaker than scattering from a barrier. It is also interesting to see here that the shift in V_t is much smaller (ΔV_t=−5 mV) and now negative. Finally, we find that cases (B) and (C), for which the impurity is placed in the oxide further away from the CNT shell, have an insignificant effect on the device performance. We would like to mention here that for a p-type device, the relative role of the positive and negative impurities would be reversed.

In this letter, we examined the role of defects (vacancies and charged impurities) in altering nanotube transistor characteristics from the ballistic limit. A single vacancy can cause drive current reduction by approximately 28%, independent of the location of the vacancy in the channel, for the device considered. While a single negatively charged impurity near the channel also decreases the drive current by a similar amount, it leads to a much larger threshold voltage shift, comparable to 40 mV (10% of the power supply). The scattering strength of the charged impurity weakens as the scatterer is placed away from the CNT channel, close to the gate electrode. For an n-type device, a localized positively charged impurity causes a much smaller drive current degradation or V_t shift (only 5 mV) compared to the negative impurity. It is quite remarkable that a single defect can cause such large degradation in drive current and threshold voltage

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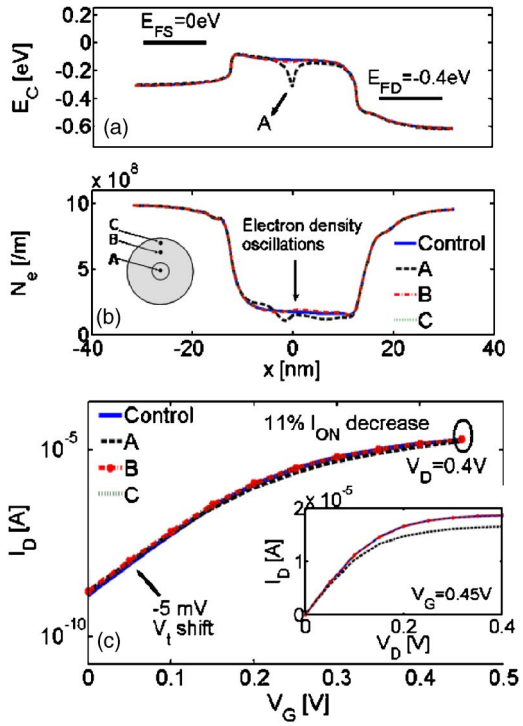


FIG. 4. (Color online) Effect of a positively charged impurity in different locations of the device. The charged impurity is placed (A) in the middle of the CNT, (B) in the middle of the oxide, and (C) near the gate electrode. (a) The conduction band of the control vs the different charged impurity cases at $V_G=V_D=0.4$ V. (b) The charge distribution along the channel for the impurity locations (A)–(C) and the same bias conditions as in (a). (c) The I_D-V_G characteristics for $V_D=0.4$ V. Inset: I_D-V_D for $V_G=0.45$ V.

shift. Design of circuits using these quasi-one-dimensional transistors should take this into consideration.

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